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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,876	03/10/2004	Anthony Dip	TPS-007	5070

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EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/797,876	DIP ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-11,13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 and 13-16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) in view of EP 0684 650 B1 to Hiroshi et al. (Hiroshi) as cited in IDS filed 03/10/2004.

Regarding claim 1, Hareland discloses a method of forming a semiconductor device (Figures 5A-5E), the method comprising: providing a substrate (502); forming a SiGe surface layer (508/520) having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24) on the substrate; depositing a high-k dielectric layer (526) onto the SiGe surface layer; and forming an electrode layer (530) on the high-k dielectric layer.

Hareland lacks disclosing forming an oxide layer between the high-k dielectric layer and an unreacted portion of the SiGe surface layer, the oxide layer being formed during one or both of said depositing and an annealing process after said depositing.

Hiroshi teaches in Figure 2B paragraphs [0043-0056] an oxide layer (thermal oxide film, SiGeO, 3a) formed between another dielectric layer (second gate insulating film, 11) and an unreacted portion of the SiGe surface layer (2B), the oxide layer being formed

during the depositing and an annealing process (Figure 3b) after said depositing (paragraph [0049]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hareland to include an oxide layer grown between the dielectric layer and an unreacted portion of the SiGe surface layer as in Hiroshi in order to modify device properties such as flatband voltage and trap charge density to improve device performance.

Regarding claim 2, Hareland in view of Hiroshi discloses the method according to claim 1 as above. Hareland also discloses the substrate provided with an initial oxide layer (Figures 5A-5E, element 506, col 9 lines 9-12) prior to forming the SiGe (508/520) surface layer.

Regarding claim 3, Hareland in view of Hiroshi discloses the method according to claim 1 as above. The modification with Hiroshi described above also includes forming the SiGe surface layer by performing thermal chemical vapor deposition, plasma-enhanced chemical vapor deposition, atomic layer deposition, or sputtering (chemical vapor deposition, paragraph [0046]).

Regarding claim 4, Hareland in view of Hiroshi discloses the method according to claim 1 as above. The modification with Hiroshi described above also includes forming the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas (paragraph [0046]).)..

Regarding claim 5, Hareland in view of Hiroshi discloses the method according to claim 4 as above. The modification with Hiroshi described above also includes the Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$ (GeH_4, paragraph [0046]).

Regarding claim 6, Hareland in view of Hiroshi discloses the method according to claim 4 as above. The modification with Hiroshi described above also includes annealing the substrate either during said exposing, after said exposing, or both during and after said exposing ("heat treatment" paragraph [0048]).

Regarding claim 7, Hareland in view of Hiroshi discloses the method according to claim 4 as above. The modification with Hiroshi described above also includes the process gas comprising a Si-containing gas (Si_2H_6, paragraph [0046]).

Regarding claim 8, Hareland in view of Hiroshi discloses the method according to claim 7 as above. The modification with Hiroshi described above also includes the Si-containing gas comprising at least one of SiH_4, Si_2H_6, or SiH_2Cl_2 (Si_2H_6, paragraph [0046]).

Regarding claim 13, Hareland in view of Hiroshi discloses the method according to claim 1 as above. Hareland also discloses the SiGe surface layer is less than about 1000 angstroms thick (less than 30 nm / 300 Å), col 10 lines 27-32).

Regarding claim 14, Hareland in view of Hiroshi discloses the method according to claim 1 as above. Hareland also discloses the SiGe surface layer is between about 10 - 300 angstroms thick (less than 30 nm / 300 Å, col 10 lines 27-32).

Regarding claim 15, Hareland in view of Hiroshi discloses the method according to claim 1 as above. Hareland also discloses the high-k dielectric layer comprises at

least one of HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, TiO_2, Ta_2O_5, Al_2O_3, or SiN (HfO_2, , ZrO_2, TiO_2, Ta_2O_5, col 11 lines 3-14).

Regarding claim 16, Hareland in view of Hiroshi discloses the method according to claim 1 as above. Hareland also discloses the high-k dielectric layer is between about 5 – 60 angstroms thick (5-15 Å, col 11 line 5).

Regarding claim 18, Hareland in view of Hiroshi discloses the method according to claim 1 as above. Hareland also discloses etching the electrode layer and the high-k dielectric layer (col 11, lines 42-46).

Regarding claim 19, Hareland in view of Hiroshi discloses the method according to claim 1 as above and Hiroshi also discloses the oxide layer formed during the annealing process by exposing the substrate to an oxygen containing gas (thermal oxidation with nitrogen or oxygen paragraph [0049]).

Regarding claim 20, Hareland discloses a method of forming a semiconductor device (Figures 5A-5E), the method comprising: providing a substrate (502); forming a SiGe surface layer (508/520) having an average Ge content less than about 10 at.% (less than 25%, col 9 lines 22-24) on the substrate; depositing a high-k dielectric layer (526) onto the SiGe surface layer; annealing the substrate (col 9 line 57); and forming an electrode layer (530) on the high-K dielectric layer.

Hareland lacks teaching one of the depositing and annealing comprising exposing the substrate to a gas to form an oxide layer between the dielectric layer and an unreacted portion of the SiGe surface layer. Hiroshi teaches annealing by exposing the substrate to an oxygen containing gas (thermal oxidation with nitrogen or oxygen

paragraph [0049]).) to form an oxide layer (thermal oxide film, SiGeO, 3a) between the dielectric layer (second gate insulating film11) and an unreated portion of the SiGe surface layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hareland to include the annealing by exposing the substrate to an oxygen containing gas as in Hiroshi in order to modify device properties including at least flatband voltage and trap charge density to improve device performance.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) in view of EP 0684 650 B1 to Hiroshi et al. (Hiroshi) as cited in IDS filed 03/10/2004 in further view of U.S. Pub. No. 2003/0218189 to Christiansen et al. (Christiansen).

Regarding claims 10 and 11, Hareland in view of Hiroshi discloses the method according to claim 1 above. Hareland lacks disclosing the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content and also lacks disclosing the SiGe surface layer comprising a graded Ge content.

Christiansen discloses a plurality of SiGe sublayers (Figure 8 layers 45, 42, 25, and 35) each with different Ge content (paragraph 82, last 3 lines) and the SiGe surface layer with a graded Ge content (Figure 9 layers 46, 37, 37 and 43, paragraph 38). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hareland to have the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content and the SiGe surface layer comprising a

graded Ge content as in Christiansen in order to reduce defects normally present in a single SiGe layer (Christiansen, paragraph 15).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,909,151 to Hareland et al. (Hareland) in view of EP 0684 650 B1 to Hiroshi et al. (Hiroshi) as cited in IDS filed 03/10/2004 as applied to claim 1 above in further view of U.S. Pat. No. 5,259,881 to Edwards et al. (Edwards).

Regarding claim 17, Hareland in view of Hiroshi discloses the method according to claim 1 as above with an Si substrate. Hareland in view of Hiroshi lacks disclosing introducing the substrate into a process chamber of one of a single wafer processing system and a process chamber of a batch-type processing system. Edwards teaches introducing a substrate into a process chamber of a batch-type processing system (col 3 lines 6-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hareland to include introducing the Si substrate into a process chamber of a batch-type processing system in order to maximize the add to the speed and flexibility of the substrate processing (Edwards, lines 14-17).

Response to Amendment

The affidavit filed on 01/26/2007 under 37 CFR 1.131 is sufficient to overcome the Interfacial Characteristics of HfO2 Films Grown on Strained SiGe by Atomic-Layer Deposition, Applied Physics Letters, Vol. 84, No. 7, 02./16/2004, pp. 1171-1173 to Cho et al (Cho). reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAM
04/16/2007

Sara Crane
Primary Examiner